

## VERIFICATION OF AMBA-AHB BASED VERIFYING IP USING UVM METHODOLOGY

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### ABSTRACT

This paper describes the verification of AMB- AHB based verifying IP using UVM (Universal Verification Methodology). AHB Is an Advanced High performance system Bus that supports multiple masters and multiple slaves. It Implements burst transfers, split transactions, single-cycle bus master handover, single-clock edge operation, wider data bus Configuration (64/128bits). Verification IP(Intellectual Property) is the one which provides a smart way to verify the AHB Components such as Master, Slave, Arbiter and Decoder. UVM is used for the verification of AHB Protocol which provides the best framework to achieve CDV (Coverage Driven Verification) which combines automatic test generation, self-checking test benches, and Coverage metrics to significantly reduce the time spent on verifying a design. An UVM test bench is composed of reusable Verification environments called VCs (verification Components). This paper examines the verification of VCs Which are structured to work with Verilog, VHDL, System Verilog and System C. AMBA Protocol based SoC it improves quality and reduces Schedule time it is the standard framework to build the verification environment waveforms, code coverage is also discussed in the paper.

**KEYWORDS:** AMBA, AHB, CDV, UVM, TLM, VC, Test Bench, Sequencer